Analog to digital converter Simulation

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***Abstract*— In this article, two models that allow for analog to digital converter (ADC) simulation are presented. One of them is a simple mathematical model taken from the literature, while the other is a circuital model. Results from simulations show nonlinear behavior, which coincides with the effects predicted in the literature. This nonlinear behavior includes both static and dynamic effects which can be measured and analyzed.**

***Keywords*— Analog to Digital Converters, nonlinearities, Models.**

1. INTRODUCTION

The actual tendency of migration towards digital signal processing systems, even for applications that were traditionally restricted to the digital domain because of their high operation frequencies and large bandwidth, has created a demand for ADCs of very high speed and low distortion. In general, high speed ADCs present strong nonlinear effects in their transfer function which cause distortion in the discrete output signal.

Several strategies for compensation of nonlinearities in ADCs have been proposed, all of them depend on the particular architecture of the ADC used. For example, a proposal oriented to successive approximation interleaved converters for OFDM (Orthogonal Frequency Division Multiplexing) is described in [1]. This proposal uses the information in the pilot tones of an OFDM frame to compensate by digital signal processing after conversion. Another alternative is described in [2], where the application of an external analog circuit as self calibrator is proposed for compensation in converters of several stages.

The availability of adequate models for ADCs is needed as a previous step to the analysis and development of compensation techniques for such converters. The goal of this article is to present the results reached in the circuital simulation of different ADC models.

In Section 2, the most common ADC architectures are briefly reviewed. In Section 3, a description of the performance parameters to characterize ADCs is performed. In Sections 4 and 5, the models of a 4 bit flash ADC and a 7 bit two stage pipeline ADC are presented, respectively, which have been used in this work. This article ends in Section 6 with some conclusions.

2. ANALOG TO DIGITAL CONVERTERS

Among the AD converters, there are different types of architectures, each having its own advantages and disadvantages. These architectures are characterized by the type of processing applied to the input signal in order to obtain the desired discrete output [3]. They can be classified, in general, as successive approximation ADCs, flash ADCs, intermediate cases between these two and sigma-delta convertes. In general, the selection of certain converter architecture is strongly dependent on the application and there is a trade-off between conversion speed and resolution, as shown in Fig. 1. Power consumption is also a key issue. In the next subsections, some well known ADC architectures are briefly reviewed.

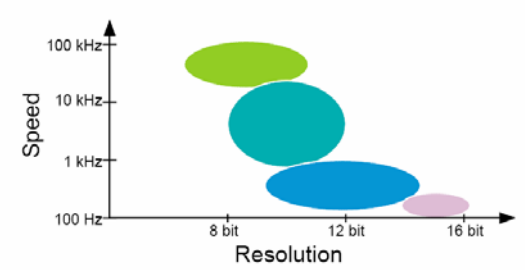

Figure 1. Speed-resolution trade-off in AD converters. Interleaved flash Converters (green), pipelined (light blue), Sigma-delta (blue) and successive approximation (pink).

2.1. Flash Converters

For the case of flash conversion, given an analog input signal, an *n* bit digital word is obtained at the output in a single clock cycle [3]. The implementation complexity of this kind of circuits is very high, and they usually require a bank of multiple resistors perfectly matched. In addition, the complexity of this structure is a function of 2^n, and therefore it increases very fast as a function of the number of resolution bits needed in the conversion. The power consumption for this kind of ADC is high and also increases with resolution. An example of this architecture is shown in Fig. 2.

2.2. Successive Approximation Converters

In the case of serial conversion by successive approximation ADCs, given an analog input signal, the corresponding *n* bit digital word is obtained in *n* clock cycles [3]. A basic description of the process involved is shown in Fig. 3. First, the sample and hold amplifier (S&H) takes a sample of the input signal at the beginning of each conversion cycle. The successive approximation register (SAR) controls the digital-to-analog converter which in turn generates the sequence of approximations. Then, a comparator compares these approximations with the output of the S&H and determines one bit of the digital output word in each clock cycle. The implementation of this type of converter is quite simple and its complexity does not depend on the resolution required in the digital word.

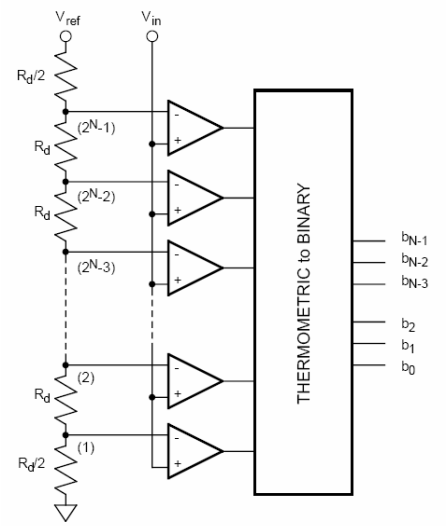

Figure 2. Structure of Flash Converters.

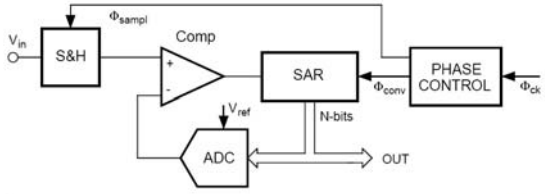

Figure 3. Structure of serial converters.

2. 3. Intermediate Solutions

There exist several architectures which represent a compromise between the two options previously mentioned [3]. One of them is the combination of *N interleaved* converters (Fig. 4). Each converter operates at a speed *N* times slower than the sampling period, and its output is then multiplexed with that of the others to obtain the sequence of digital words at full speed. The natural advantage of this scheme is that it allows to multiply the effective sampling speed by *N* without the need of faster converters. Among the inconvenients, it's worth mentioning that if there is an error in any of the conversion channels, then every N commutation cycles the signal obtained differs from the correct value. This gives origin to a distortion component in the frequency *fs/N*, where *fs* is the sampling frequency. Furthermore, the errors that cause this effect, such as gain and offset errors, are very common in practice.

Another alternative is the so called *pipelined* converter (Fig. 5), in which the bits are obtained in blocks of equal length from the most significant bit (MSB) to the least significant bit (LSB). Then, the conversion is achieved in as many clock cycles as blocks in which the digital word is divided into. However, while the information corresponding to a sample is being processed in an intermediate block, the previous block is already processing the information corresponding to the next sample. Therefore, after an initial latency of *x* samples, where *x* is the number of blocks, the conversion of successive samples is obtained at a rate of one output digital word for clock cycle.

2.4. Sigma-Delta Conversion

Sigma-Delta converters (SDC) combine low resolution convertion with oversampling and noise shaping. In this manner, it is possible to obtain a large dynamic range with low cost and low power consumption. In the case of one bit

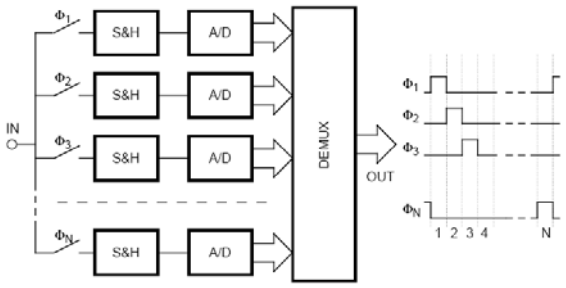

Figure 4. Structure of Interleaved Converters.

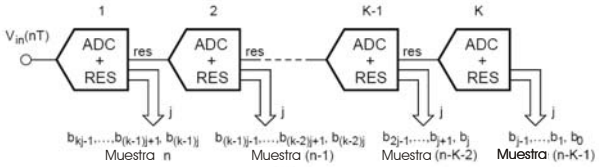

Figure 5. Structure of Pipelined converters.

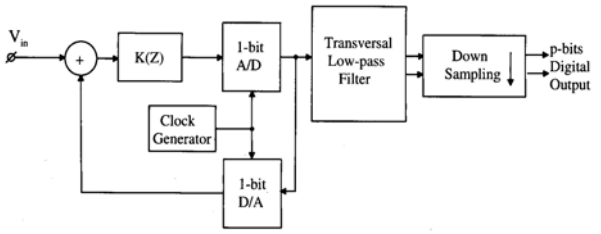

Figure 6. Sigma-Delta AD converter.

conversion, the inherently high linearity of both the ADC and DAC (Digital to Analog Converter) reduces distortion to a minimum.

For a 1 bit first order SDC, the procedure is as shown in Fig. 6. First, the input signal is applied to an integrator, and the result is quantized using a comparator followed by a latch. The output of the quantizer is then fed back to the input through a DAC, and subtracted from the input signal before integration. After the loop, a low pass filter is used to reject the out of band quantization noise, and after a decimation process, a multi-bit signal with improved dynamic range is provided [3].

Addition of integrators in the feedback loop increase the noise shaping order, thus enhancing the dynamic range of the output digital signal. However, care must be taken for orders higher than two as stability problems can arise. Also, the oversampling required for the noise shaping process is usually larger than 10. Hence, the achievable word rate is reduced by this factor.

Independently of the type of converter being used, when the AD conversion must be carried out at high speed, there will be nonlinear effects at the output which must be compensated for. These nonlinearities have their origin in the different subsystems that compose the converter, and each one of them alters the output signal determining a joint response. The result is a harmonic distortion that deteriorates de dynamic range in the frequency band of interest of converter, raising the noise floor.

3. PERFORMANCE PARAMETERS IN ADCs

In this section some performance parameters often used in converters are described. This allows one to determine how

close to the ideal conditions does a particular structure operate. Some of these parameters characterize the nature of the static nonlinear behavior of an ADC, and others are used to test its dynamic performance [3].

3.1. Parameters that characterize the static nonlinear behavior of an ADC

The integral nonlinearity (INL): is the difference between the ideal analog voltage that should cause the transition from output code k-1 to code k, and the real voltage that actually causes that transition. Its calculation is done after correcting for gain and offset. This correction is performed so as to minimize:

$$\varepsilon(k) = T_k - G.T[k] - V_{OS}$$

where T_k is the analog voltage that would cause a transition in an ideal ADC and $T[k]$ is the voltage that actually causes that transition. Then, the integral nonlinearity (as a percentage of the converters full range, after correcting for gain and offset) can be expressed as follows:

$$INL[k] = \frac{100.\varepsilon[k]}{2^B.Q}$$

where Q is the analog voltage equivalent to a LSB, and B the number of resolution bits in the converter.

The differential nonlinearity (DNL): is the real voltage step between two successive transitions $W[k]$ and Q, which is the value of each step in an ideal ADC. For that reason it can also be defined as $INL[k+1]$-$INL[k]$. In general, the DNL is expressed referred to Q:

$$DNL[k] = \frac{W[k] - Q}{Q}$$

A missing code is considered to exist if:

$$DNL[k] \le -0{,}9$$

The input-output graphics for an ideal converter (dashed line) and a real ADC (full line) are shown in Fig. 7.

3.2. Parameters to test the dynamic performance

Signal to Noise Ratio (SNR): In an ideal ADC, the SNR is the ratio between the power of a sinusoidal input signal and the power of the quantization noise at the output of the converter. It can be shown that for this case the SNR is:

$$SNR[dB] \cong 6.n + 1.72 \qquad (1)$$

where n is the number of bits of resolution in the converter.

Spurious Free Dynamic Range (SFDR): For a pure sinusoidal input signal of specified amplitude and frequency, the SFDR is defined as the ratio between the amplitude of the output signal at the input frequency, and the amplitude of the largest harmonic component.

Total Harmonic Distortion (TDH): The sum of the powers of all harmonic distortion components in the spectrum of the output signal of an ADC (including its alias), defined for a pure sinusoidal input signal of specified amplitude and frequency. In general, the THD can be approximated by the power from the second to the tenth harmonics. Sometimes, the THD is expressed as the ratio in dB referred to the power of the output signal at the input frequency.

THD is a convenient figure of merit for evaluation of the nonlinear behavior in ADCs, given the fact that nonlinear effects are closely related to the harmonic distortion terms in the output signal. This means that minimizing the THD leads to a reduction of nonlinear distortion, and so to linearization.

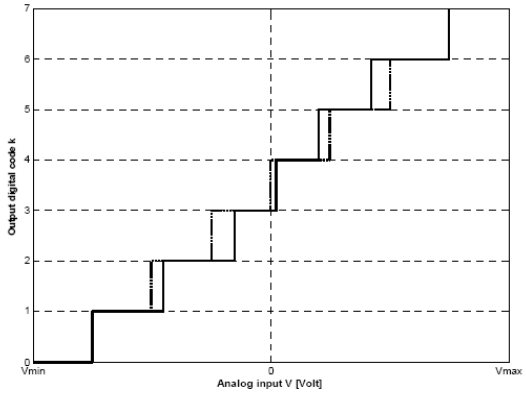

Figure 7. Input-output plot for an ideal ADC (dashed line) and for a real ADC (full line).

Effective Number Of Bits (ENOB):It is the number of bits in an ideal ADC for which the RMS value of the quantization noise is equal to that of noise plus distortion in the ADC under test. The ENOB can be extracted from the following equation derived from (1):

$$SINAD[dB] \cong 6.ENOB + 1.72$$

For an ideal ADC, SNR takes into account only quantization noise. Now, for a real ADC, SNR must be replaced by SINAD (Signal to Noise and Distorsion Ratio), where SINAD takes into account quantization noise plus all errors due to the non ideal behavior of the converter and nonlinear distortion. Thus, sum of errors that are not present in an ideal converter reduces the SINAD or, equivalently, reduce the ENOB. Then the ENOB is the effective number of bits referred to the number of bits in an ideal ADC.

4. MODELS AND SIMULATIONS OF FLASH CONVERTERS

In this section we analyze the performance of flash ADC models. In particular, two models that offer a good representation of this device will be considered. The first model is the circuital model of a 4 bit flash ADC, where input-output data are obtained by means of Spice simulations and then exported to MATLAB for processing. The schematic is shown in Fig. 8. The comparators used (T1720) are taken from the software library, where the behavioral model is provided by the manufacturer (Phillips). The resistors used for the reference ladder are discrete components with a 5% tolerance on the nominal value.

The second is a mathematical model proposed in the literature [4], where even and odd harmonics of the input signal are created using hyperbolic functions, and then the sum is applied to the input of an ideal quantizer (Fig. 9.). The parameters of this model, such as the amplitude and decaying ratio of the harmonics, should be determined by measurements on a real ADC. In fact, the coefficients of the hyperbolic functions can be found in the literature for some ADCs [4]. For example, for a 4 bit ADC the coefficients are a= 0.1, b= 0.0018, c= 0.87, d= 0.11 and k= 0.93. For a 6 bit ADC, the parameters that best fit the spectrum measurements are a= 0.011, b= 0.l, c= 0.6, d= 0.011 and k= 1. The advantage of this model is that the resolution of the converter can be arbitrarily changed by simply specifying the number of bits needed in the output digital word. Its major drawback is that a very intensive experimental work is required to adjust the amplitude and decaying rate of the

harmonics in the model based on measurements of real converters. In addition, this work has to be redone every time the ADC resolution is changed.

A comparison on the behavior of the two models was performed. For that purpose, a sinusoidal input of 500 kHz was used in Spice as stimulus for the 4 bit flash ADC circuital model. Both input and output obtained were exported to MATLAB, and after applying the same input signal to the mathematical and ideal models, the spectrum of the output signal for the three converters was computed (Fig. 10.).

It can be seen from the figure that the ideal converter has spectral components only in the odd harmonics of the input signal. However, both the mathematical and the circuital model have spectral components in even and odd harmonics of the input signal, although its amplitudes differ.

SNR was also computed for each converter as a performance measurement. The SNR is the ratio between the power of the input signal and the power of the error signal between input and output. From (1), we know that the theoretical value of the SNR for a 4 bit ideal ADC is about 25.72 dB. The results obtained were:

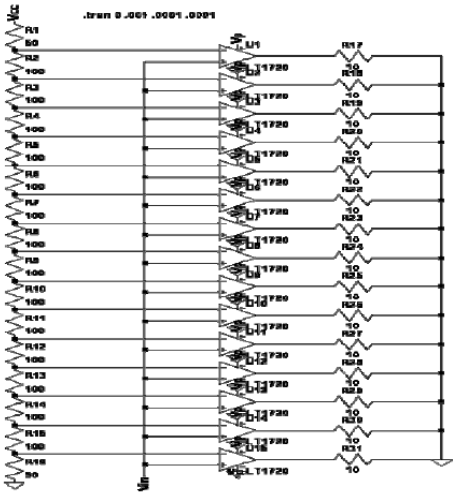

Figure 8. Circuital model of a 4 bit flash ADC.

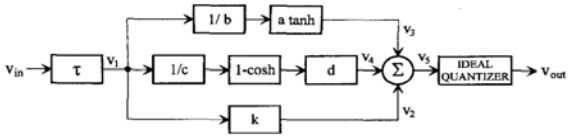

Figure 9. Mathematical model of an ADC.

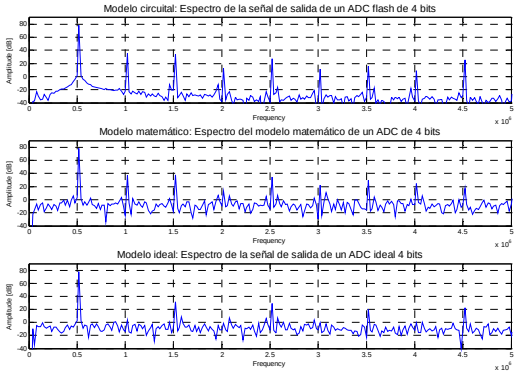

Figure 10. Output spectrum of the circuital model of an ADC (top), the mathematical ADC (medium), and an ideal ADC (bottom).

$SNR_{Ideal} = 25{,}6536\,[dB]$, $SNR_{Mathematical} = 25{,}3408\,[dB]$, $SNR_{Circuital} = 24{,}9403\,[dB]$

These results are as expected, given the fact that the difference between the theoretical value of the SNR and the one obtained by simulation for the ideal ADC is small and can be explained by the approximation error. For the cases of the circuital and mathematical models, a loss in the SNR was expected due to the nonlinear effects present in these converters. These nonlinear effect cause distortion, which added to the quantization error gives a reduction in the SNR.

Next, an input-output plot was obtained for the three models, in order to be able to visualize the nonlinear effects which cause this reduction in the SNR (Fig. 11).

It can be seen that the input-output relation for the mathematical model differs from the ideal, but always in a similar manner. This would imply the presence of static nonlinearities. On the other hand, for the circuital model the corresponding input-output relation does not only differ much more from the ideal than in the previous case, but also that the curve is not unique. This can be interpreted as a memory effect, i.e., the system has dynamic nonlinearities.

As mentioned before, INL can be defined as the difference between the analog voltage producing a level transition in an ideal ADC and the voltage that causes that transition in a real device. For transition *k*:

$$INL(k) = V_{ideal}(k) - V_{real}(k)$$

This can be seen as the difference in the input-output plot for the three ADC models. It is clear that a reduction in INL leads to a behavior closer to the ideal.

Therefore, a model of the INL for the converter to be compensated is of great importance in an extern compensation scheme, because it is directly related with the distortive effects present in the ADC. The simulated voltages that produce a level transition in an ideal ADC and in the circuital model of a 4 bit flash ADC are shown in the upper part of Fig. 12. The lower part of the same figure shows the normalized INL corresponding to each transition. It can be seen that for this ADC model, transitions in one direction produce different values of INL than the ones in the opposite direction.

5. MODELS AND SIMULATIONS OF PIPELINED CONVERTERS

5.1. Description

As mentioned before, a pipelined ADC consists of a set of successive stages connected by S&H amplifiers. The first stage performs the coarse quantization of the input signal,

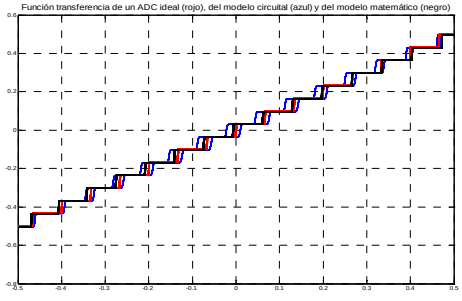

Figure 11. Input-output graphic for the three ADC models.

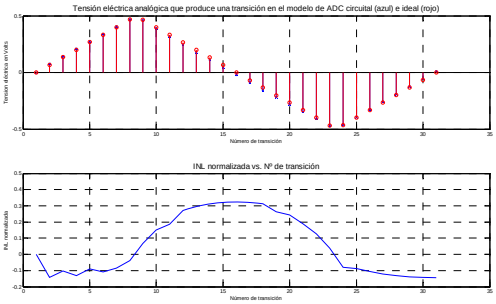

Fig. 12. Analog voltage producing a transition in the real and ideal ADCs (top) and normalized INL (bottom).

and the following stages carry out the fine quantization using the residue signal from the precedent stage. The digital words obtained in each stage are then combined to compose the complete output word. As a consequence, a great bit resolution can be achieved using lower resolution ADCs (Fig. 13). Each stage of a pipelined converter is composed of a S&H amplifier, a *B* bit ADC, a DAC (Digital to Analog Converter), a subtracting circuit to calculate the residue, and a residue amplifier (Fig. 14).

The residue is the difference between the analog input voltage to the conversion stage, and its quantized version obtained with the DAC from the digital output word of the AD sub-converter. Ideally, the residue takes values in the [0, LSB] range, and then the output of each stage should be the residue amplified by 2^B. Such signal would be proportional to the residue, but in the initial input range. This way, the residue can be quantized in each stage with an ADC *exactly equal* to the one used in the previous stage.

In practice, the residue signal (which determines the fine quantization) is affected by several sources of error. Some of them are offset in the amplifier, gain errors, ADC nonlinearities and DAC imperfections. These errors can cause total or partial saturation of the signal, distortion and loss of information. However, if one reduces the gain of the amplifier at the output of each stage to 2^{B-1}, the range of the resulting signal is divided by two and some errors can be detected and corrected by post-processing. The cost of this solution is the loss of one resolution bit per stage. In general, errors due to offset and subconverter nonlinearities can be successfully corrected. Gain errors, on the other hand, can cause missing codes and their correction is not trivial [5]. An example of missing codes caused by inter-stage gain errors is illustrated in Fig. 15.

5.2. Circuital model of a 7 bit pipelined ADC

Using the 4 bit flash ADC model previously described, the circuital model of a 7 bit two stage pipelined ADC was developed. For that purpose, the circuital model of the flash converter was used at the input of the system to perform the coarse quantization of the input signal. In this manner, a 4 bit digital word representing the analog input signal is obtained at the output of the first stage.

Then, the quantized signal is reconverted to the analog dominion (DAC) and the result is subtracted from the input signal. At the output of the subtracting circuit the residue signal is obtained. This signal is the difference between the input signal and its 4 bit quantized version.

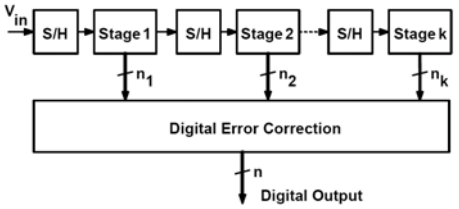

Figura 13. Block diagram of a pipelined ADC.

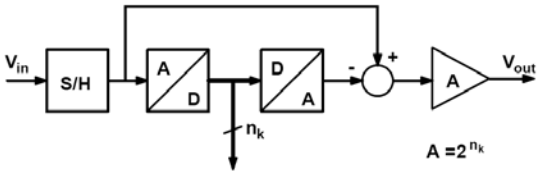

Figure 14. Stage of a pipelined ADC.

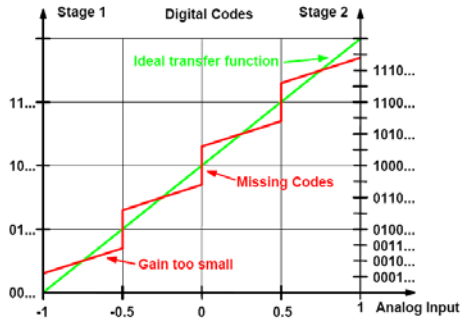

Fig. 15. Gain errors and missing codes.

If the residue signal is perfect, when amplifying by 2^B the result is a proportional signal but in the range $[0,2^B]$. If this signal is then fed to a 4 bit flash ADC equal to the one used in the first stage, another 4 bit digital word is obtained as fine quantization. The result from combining both coarse and fine quantization digital words is a quantization of 8 bits of resolution.

However, due to the presence of errors, the output range of the first stage must be reduced by two in order to be able to correct them. Because of this, the residue from the coarse quantization is amplified by $2^{B-1}=8$ instead, obtaining a signal proportional to the residue but in the range [0, 8.LSB]. As a result, a 3 bit fine quantization is achieved, determining a total word length of 7 bits.

The scheme of the 7 bit two stage pipelined converter simulated in Spice is shown in Fig. 16. The simulated converter consists of two stages composed of a 4 bit flash subconverter and a DAC. At the output of the first stage, a subtracting circuit to compute the residue and an amplifier are used. The time domain signals obtained in Spice were then exported to MATLAB for processing and ADC characterization. The calculation of the INL was also carried out for this case (Fig. 17), which is sufficient to represent the nonlinear behavior of the converter.

As can be seen from the figure, the INL has three components: a smooth variation, sawtooth-like variations and noise peaks. These results are similar to those found in the literature [6] for a commercial 12 bit pipelined ADC. The slow variation, which may be approximated by a polynomial function, is the only component present in the 4 bit flash ADC previously characterized. The other variations

are related to gain and offset errors between the two stages of the converter.

The SNR was also computed for both converters as a performance measurement. From equation (1) it follows that the theoretical SNR for an ideal 7 bit ADC is about 43.72 dB. The results from simulation are:

$$SNR_{Ideal} = 43{,}9734 \ \ [dB], \ SNR_{Circuital} = 39{,}4157 \ \ [dB]$$

These results are as expected. For the ideal ADC, the difference between the theoretical SNR value and the one obtained from the simulation is small and can be explained by the approximation error. For the circuital model, a loss in the SNR was expected due to the nonlinear effects present in the ADC. Note that an ENOB=6.28 is obtained, which seems more than reasonable.

6. CONCLUSIONS.

In this work, numerical simulations of two ADC models are presented. In all cases, results show great similarities with the characteristics presented in the literature. These simulations will be the base for analysis of ADC compensation schemes that will be presented in future papers. In the near future, the circuital models will be further improved and compared with actual measurements. In particular, a Sigma-Delta circuital model is being developed at transistor level in 180nm CMOS technology, so that the chip can be made and measured to validate simulation results.

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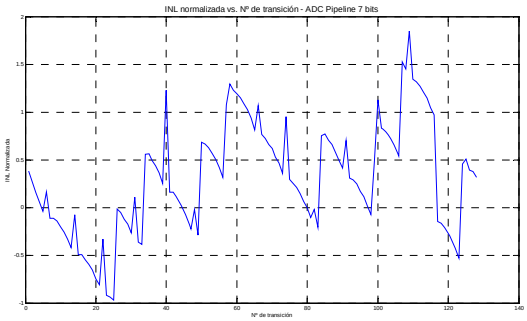

Fig. 17. INL of the pipelined converter model.

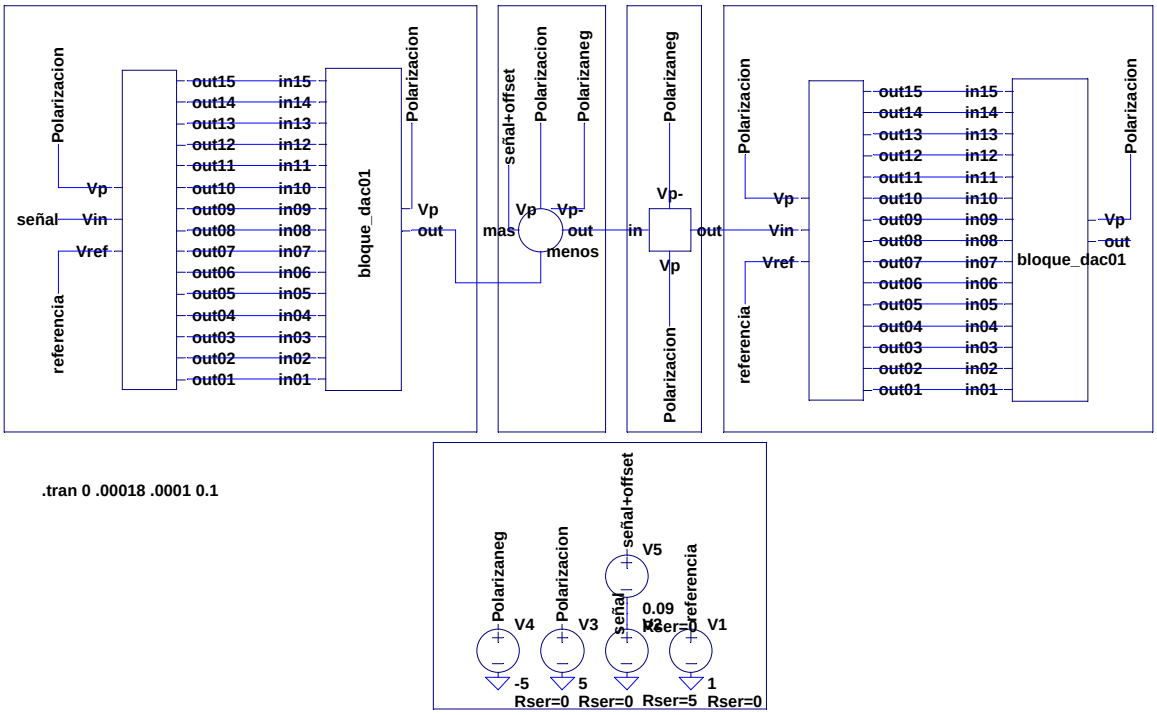

Fig. 16 Circuital model of a pipelined converter